

12 GS/s Digital-to-Analog Converter

TDAC-2000 Data Sheet



TDAC-2000

General Description

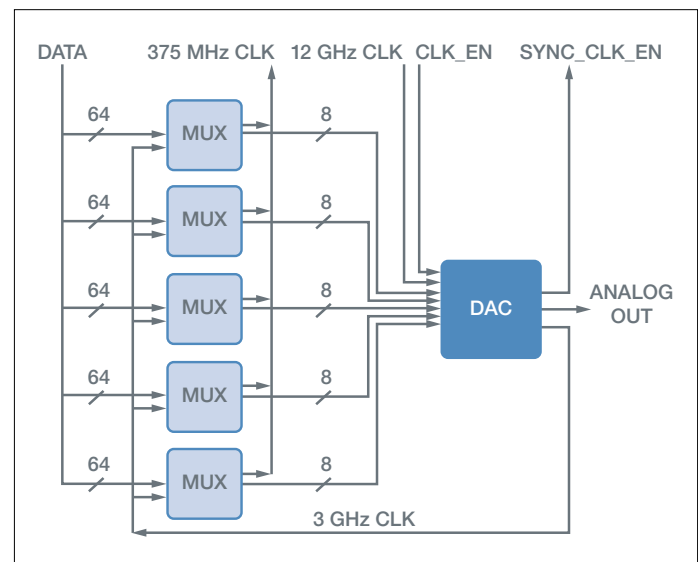
The TDAC-2000 is a single-channel waveform generation engine comprised of multiplexers and a digital-to-analog converter operating at 12 GS/s (Gigasamples per second). Data is supplied to the multiplexers via 320 data lines at 375 Mb/s (120 Gbps aggregate rate) using clocks generated by the DAC and multiplexers from a 12 GHz input clock. The TDAC-2000 can be used for application prototype development and can also be deployed in embedded systems where the form factor is acceptable. For customers who need to meet specific form, fit or function requirements, Tektronix Component Solutions can utilize the DAC to create an integrated solution.

Features & Benefits

- Waveform generation at 12 GS/s
 - World's fastest commercially available 10-bit DAC module
- Single-ended CMOS parallel interface
 - Easy interfacing to FPGAs
- Streaming at 120 Gbps
 - Module is able to sustain full-bandwidth streaming
- Provides customer access to Tektronix DAC technology
 - Complete packaged and validated design speeds time-to-market

Applications

- Digital RF Memory (DRFM)
- Radar simulation
- SIGINT, ELINT, COMINT
- Communications
- Electronic warfare
- Embedded ATE



Block Diagram

Theory of Operation

The TDAC-2000 consists of a high speed, 10-bit DAC with a built-in 4:1 multiplexer fed by five 8:1 multiplexers. The DAC chip itself generates clocking for the multiplexers by dividing the high speed system clock by four and providing multiple outputs for the multiplexer chips. These chips, in turn, divide their input clock by eight and provide the divided down-clock through the module connectors for clocking data input.

Start and stop of the analog waveform output is accomplished using the CLK_EN signal to the DAC chip. This is a high speed external signal to the board (differential pair through SMP connectors) that is set high to enable the clock tree in the DAC and multiplexers to operate and output data. The clock state machine in the DAC is reset on CLK_EN so the chip always starts in the same state.

Several mechanisms for adjusting timing are built into the system. The main system input clock (12 GHz) can be adjusted via the CLK_I_MULT and CLK_Q_MULT registers through 180 degrees of phase, allowing precise timing of the output and alignment of multiple DAC outputs. The output clocks from the DAC that drive the multiplexers can be adjusted in quarter-cycle increments to facilitate data alignment at the inputs of the multiplexers. Data alignment from the multiplexer to the DAC inputs can be adjusted using a variable delay on each of the multiplexer outputs (0-1400 ps, in 30 ps increments). In practice it has not been found necessary to use either of the data alignment adjustments since care was taken in matching

lengths of all clock and data lines. Finally, adjustment of the multiplexer output clocks (used to time input data) is possible via the AdjustStrobe register in the multiplexer, which effectively skips one high speed clock cycle in output clock generation with each register write. The state of this alignment is maintained even when the clock is disabled via CLK_EN.

Alignment of multiple DACs is facilitated by a SYNC_CLK_EN output from the DAC. This signal is synchronized to the high speed system clock, and allows a CLK_EN signal applied to one DAC to be forwarded to a second DAC without having to precisely match cables.

The TDAC-2000 also has two programmable marker outputs whose timing and amplitude can be adjusted independently of the DAC analog output. Use of each marker removes one LSB of output adjustment from the DAC (i.e., using two markers means there are 8 bits of adjustment on the DAC output).

Electrical Specifications

Channels	1
Physical bits	10
Sample rate	12 GS/s
SFDR	> 45 dB to 2 GHz
Non-Linearity	0.2% of full scale DC DNL, 0.4% of full scale DC INL
Analog Output Bandwidth	8.5 GHz 3 dB bandwidth

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_p	Power supply voltage, +3.3 V	Min -0.3 Max +3.6	V
V_n	Power supply voltage, -5.1 V	Min -7.0 Max +0.3	V
V_{pp}	Clock input, either pin of differential pair	2	V

DC Electrical Characteristics

(Global Conditions: $T_A = 0^\circ\text{C}$ to $+50^\circ\text{C}$. Typical values at $T_A = +25^\circ\text{C}$ unless otherwise noted.)

Power Supply

Parameter	Conditions	Symbol	Min	Typical	Max	Units
Power Supply Voltage, +3.3 V		V_p	3.0	3.3	3.4	V
Power Supply Current, +3.3 V		I_p		3.6	4.7	A
Power Supply Voltage, -5.1 V		V_n	-5.25	-5.1	-5.0	V
Power Supply Current, -5.1 V		I_n		1.5	1.7	A
Data Input Reference Voltage ¹		V_{ref}	1.8		3.3	V

Inputs

Parameter	Conditions	Symbol	Min	Typical	Max	Units
Clock In ^{2,3}		V_{pp}	400		1000	mV
Digital Data In, High Level	Reference voltage 1.8 V	V_{ih}	1.2			V
Digital Data In, Low Level	Reference voltage 1.8 V	V_{il}			0.6	V
Reset 1:0	High true CMOS			3.3		V
Clock Enable In, Differential		V_{idiff}	± 200	± 400	± 900	mV
Clock Enable In, Common Mode		V_{icm}	-1.5	-1.3	-1.1	V

Outputs

Parameter	Conditions	Symbol	Min	Typical	Max	Units
Analog Out, Differential, Per Side into 50 ohms		V_{out}	± 0.27	± 0.5	± 0.53	V
Clock Out, Differential		V_{odiff}	± 280	± 370	± 450	mV
Clock Out, Common Mode		V_{ocm}	1.0	1.2	1.4	V
Sync Clock Enable, Differential	100 ohms V_p to V_n	V_{odiff}	± 400	± 500	± 610	mV
Sync Clock Enable, Common Mode	100 ohms V_p to V_n	V_{ocm}	-1.5	-1.35	-1.31	V

Note 1: Input data threshold is set to $V_{ref}/2$

Note 2: Clock is AC coupled through $83\text{ pF} + 100\text{ nF}$ (16 kHz to 12 GHz)

Note 3: Differential swing for clock input is 400-1000 mVpp. One input may be terminated and the other input driven single-ended at this level if necessary.

AC Electrical Characteristics

(Global Conditions: $V_{CC} = +10.8$ to $+13.2$, $T_A = 0^\circ\text{C}$ to $+50^\circ\text{C}$. Typical values at $T_A = +25^\circ\text{C}$, $V_{CC} = +12$ unless otherwise noted.)

Inputs

Parameter	Conditions	Symbol	Min	Typical	Max	Units
Clock In					12	GHz
Clock Enable In				10	12	Mbps
Digital Data In					375	Mbps

Outputs

Parameter	Conditions	Symbol	Min	Typical	Max	Units
Analog Out Bandwidth				5	8.5	GHz
Sync Clock Enable Out					12	GHz

Environmental Specifications

Air flow over module

- > 400 LFM

Operating Temperature

- 0 to 50°C

Storage Ambient Temperature

- -40 to 71°C

Relative Humidity

- 0 to 90% at 30°C

Mechanical Specifications

Board dimensions

- 4.40 in. x 4.20 in., thickness 0.124 in. \pm 10%
- 0.508 in. \pm 0.016 in. front side height (including heatsinks)
- 0.128 in. +0.003/-0.001 in. back side height

Mounting holes

- Four 0.125 in. diameter, 0.250 in. plated pads

Extraction holes

- Six 4-40 threaded pemnuts for board removal screws to minimize flexure

Connectors

- Three Samtec QSH-090-01-F-D-A, 180 pins
- 12 Tensolite P797 SMP right-angle coax³
(differential DAC out, 12 GHz clock in, clock enable in, sync clock enable out, 2 x marker pulse out)
- One 10-pin JTAG connector

Heat Sinks

- DAC: Alpha Novatech MD30-10B, 30x30x10 mm
- MUX: Alpha Novatech LPD19-10B, 19x19x10 mm

Thermal Resistance

- Junction to back side of Heat Sink
- DAC: 1.3 C/W
- MUX: 2.7 C/W

Power Dissipation (Typical)

- DAC: 7 W
- MUX: 3 W (each)

About Tektronix Component Solutions

With four decades of expertise, a talented in-house engineering team, a lean US-based manufacturing facility, advanced test capabilities and DSCC-suitable labs, Tektronix Component Solutions brings performance, reliability and quality to component design, assembly and test.

Originally created in 1970 as the Hybrid Components Organization within Tektronix, the group was formed to supply high-performance components for Tektronix high-speed measurement equipment, a charter we continue to fulfill today.

In 1994, our organization was spun out as a joint venture between Maxim and Tektronix. As Maxtek, we began to apply our expertise in the design, assembly and test of demanding microelectronics for customers in a variety of industries.

Reacquired by Tektronix in 2000 and renamed Tektronix Component Solutions in 2010, our organization continues to provide a full range of design, assembly and test services to those requiring components for demanding applications.

We are headquartered in Beaverton, Oregon, with additional sites in Orlando, Florida and Phoenix, Arizona.

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